Fiabilité électroniq

A New Characterization Technique for Extracting Parasitic Inductances of SiC Power MOSFETs in Discrete and Module Packages Based on Two-Port S-Parameters Measurement

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The parasitic inductances of silicon carbide (SiC) power MOSFETs have a major influence on their operation and circuit performance. They incur negative effects such as switching oscillations, power losses and electromagnetic interference (EMI) noise. This paper introduces a new technique to accurately characterize the parasitic inductances of SiC power MOSFETs in both discrete packages and power modules based on two-port S-parameters measurement. By treating a power MOSFET as a two-port network,

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METHOD FOR GROWING GaN CRYSTAL AND C-PLANE GaN SUBSTRATE

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The main object of the present invention is to provide a novel method for growing a GaN crystal suitable as a material for a GaN substrate including a C-plane GaN substrate. Another object of the present invention is to provide a novel C-plane GaN substrate which can be suitably used for manufacturing a nitride semiconductor device, etc. Provided is a method for growing a GaN crystal, the method comprising: a first step for preparing a GaN seed having a nitrogen polar surface; a second step for disposing a pattern mask on the nitrogen polar surface of the GaN seed, wherein the pattern mask is provided with a periodic opening pattern which is composed of linear openings and includes intersections, and the pattern mask is disposed such that the angle between the longitudinal direction of at least a portion of the linear openings and the direction of the line of intersection between the nitrogen polar surface and the M surface is within ±3°; and a third step for ammonothermally growing the GaN crystal on the nitrogen polar surface of the GaN seed through the pattern mask, wherein a gap is formed between the GaN crystal and the pattern mask. A novel C-plane GaN substrate which can be suitably used for manufacturing a nitride semiconductor device, etc is also provided.

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STACKING FAULT-FREE SEMIPOLAR AND NONPOLAR GAN GROWN ON FOREIGN SUBSTRATES BY ELIMINATING THE NITROGEN POLAR FACETS DURING THE GROWTH

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Methods and structures for forming epitaxial layers of Ill-nitride materials on patterned foreign substrates with low stacking fault densities are described. Semipolar and nonpolar orientations of GaN that are essentially free from stacking faults may be grown from crystal-growth facets of a patterned substrate. Etching can be used to remove stacking faults if present. Crystal growth with an impurity can eliminate crystal growth from a facet that is responsible for stacking fault formation and permit substantially stacking-fault-free growth of the Ill-nitride material.

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GaN-based Field-Effect Transistors with Laterally Gated Two-Dimensional Electron Gas

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In this letter, we report on GaN-based field-effect transistors with laterally gated two-dimensional

electron gas (2DEG). The drain current of the transistor is controlled solely by modulating the width of the 2DEG between buried gates. The lateral Schottky gate contact to the GaN channel layer enhances electron confinement by raising electrostatic potential below the 2DEG, improving isolation between the source and drain. Complete elimination of a top-contact gate reduces the density of trapped

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Zero-Voltage Switching Full-Bridge T-type Isolated DC/DC Converter with Wide Input Voltage Range and Balanced Switch Currents

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With the development of silicon carbide (SiC) power devices, the circuit structure of power converter for high voltage applications would be simpler and more compact because the two-level based topologies become applicable. This paper proposes a full-bridge (FB) T-type isolated DC/DC converter for the applications with high input voltage and wide input voltage range. The proposed converter is composed of four main power switches with high voltage stress (SiC MOSFET) and four auxiliary power swit

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METHOD OF INCREASE OF THRESHOLD BARRIER VOLTAGE OF GAN TRANSISTOR

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FIELD: electricity.SUBSTANCE: method of increasing the threshold barrier voltage of a transistor based on gallium nitride (GaN), which includes creating gate p-GaN mesa on the surface of the silicon wafer with epitaxial heterostructure of GaN/AlGaN/GaN type, inter-instrument mesa-isolation, forming ohmic contacts to the areas of the transistor drain and source, forming a two-layer resistive mask by lithographic methods, cleaning of the surface of the semiconductor, deposition of thin films of gate metallization, removing of the plate from the vacuum chamber of the evaporator, removal of the resistive mask, prior to the evaporation of thin films of gate metallization the plate is subjected to treatment in an atmosphere of atomic hydrogen for t=10-60 seconds at a temperature of t=20-150°C and flow density of hydrogen atoms on the surface of the plate, equal to 10-10at. cmc.EFFECT: increase in the threshold barrier voltage of the GaN transistor when applying barrier metal films to the p-GaN gate area with a high electronic work function.5 cl, 3 dwg

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Integrated ESD Protection Circuit for GaN Based Device

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The present disclosure relates to an electrostatic discharge (ESD) protection circuit integrated with a gallium nitride (GaN) based transistor and configured to clamp a gate input voltage of the gallium nitride (GaN) based transistor during an ESD surge event, and associated methods. In some embodiments, the ESD protection circuit includes a first ESD protection stage and a second ESD protection stage connected between a gate terminal and a source terminal of the GaN based transistor. The first ESD protection stage includes a first plurality of GaN based gate-to-source shorted transistors connected in series and further connected to a first terminal of a first resistor. The second ESD protection stage is connected to the first ESD protection stage in parallel. The second ESD protection stage comprises a first GaN based shunt transistor having a gate terminal connected to the first terminal of the first resistor.

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METHOD FOR STATISTICALLY ANALYZING PROCESS PARAMETERS OF GAN

DEVICE BASED ON LARGE-SIGNAL EQUIVALENT CIRCUIT MODEL

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Provided is a method for analyzing process parameters based on a GaN device equivalent circuit model, comprising: step I: establishing a GaN device small-signal equivalent circuit model to extract small-signal model parameters; step II: establishing a GaN device large-signal equivalent circuit model to extract large-signal model parameters, i.e., nonlinear current source model parameters and nonlinear capacitor model parameters; step III: tuning and optimizing the large-signal model parameters with the goal of measured microwave properties of the device; and step IV: extracting process parameters of multiple batches of GaN devices based on the established large-signal model, and statistically analyzing the process parameters. By means of the method for statistically analyzing process parameters of a GaN device model, first establishing a GaN device small-signal equivalent circuit model, then establishing a GaN device large-signal equivalent circuit model associated with process parameters, and finally modeling multiple batches of devices to obtain statistical distribution of the process parameters are beneficial to device yield analysis and process parameter optimization.

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Silver sintering die attachment for power chip in power module

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Higher operation temperature and high current density requests of new generation power devices make it is more and more complicated to meet the quality requirements for power electronic modules. Especially the (silicon carbide) SiC and gallium nitride (GaN) power device lead to the maximum operation temperature more than 200°C. Solder should be an issue for die bond material, and silver sintering material can satisfy the demands of power modules in the future. Silver sintering can be the candida

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GaN-on-Si SEMICONDUCTOR DEVICE STRUCTURES FOR HIGH CURRENT/ HIGH VOLTAGE LATERAL GaN TRANSISTORS AND METHODS OF FABRICATION THEREOF

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A GaN-on-Si device structure and a method of fabrication are disclosed for improved die yield and device reliability of high current/high voltage lateral GaN transistors. A plurality of conventional GaN device structures comprising GaN epi-layers are fabricated on a silicon substrate (GaN-on-Si die). After processing of on-chip interconnect layers, a trench structure is defined around each die, through the GaN epi-layers and into the silicon substrate. A trench cladding is provided on proximal sidewalls, comprising at least one of a passivation layer and a conductive metal layer. The trench cladding extends over exposed surfaces of the GaN epi-layers, over the interface region with the substrate, and over the exposed surfaces of the interconnect layers. This structure reduces risk of propagation of dicing damage and defects or cracks in the GaN epi-layers into active device regions. A metal trench cladding acts as a barrier for electro-migration of mobile ions.

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RELIABLE ELECTRICAL CONTACTS FOR HIGH POWER PHOTOCONDUCTIVE SWITCHES

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A photoconductive switch consisting of an optically actuated photoconductive material, e.g. a wide bandgap semiconductor such as SiC, situated between opposing electrodes. The electrodes are created using various methods in order to maximize reliability by reducing resistive heating, current concentrations and filamentation, and heating and ablation due to the light source. This is primarily accomplished by the configuration of the electrical contact geometry, choice of contacts

metals, annealing, ion implantation, creation of recesses within the SiC, and the use of coatings to act as encapsulants and anti-reflective layers.

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